512K x 8 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

NOVEMBER 2016

FEATURES

- High-speed access time: 55ns, 70ns
- CMOS low power operation
  - 36 mW (typical) operating
  - 9 µW (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
  - 1.65V – 2.2V V_{DD} (IS62WV5128ALL)
  - 2.5V – 3.6V V_{DD} (IS62WV5128BLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial temperature available
- Lead-free available

DESCRIPTION

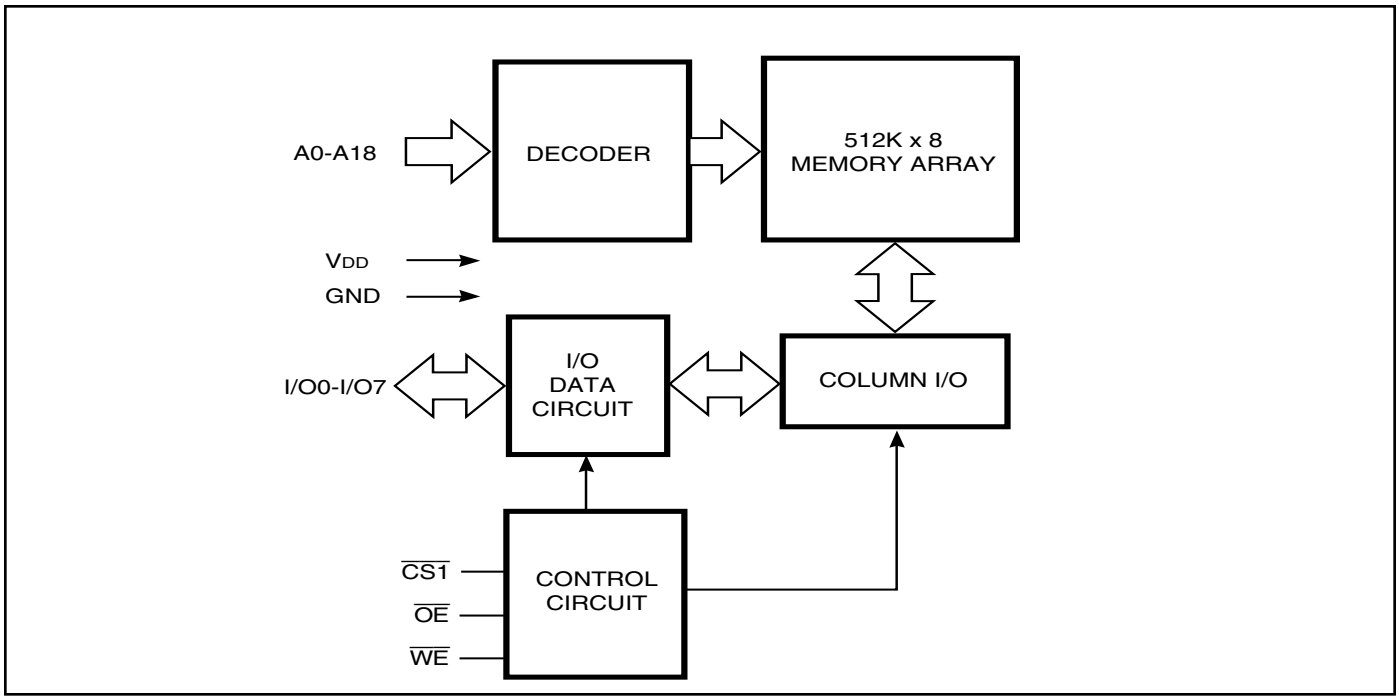
The ISSI IS62WV5128ALL / IS62WV5128BLL are high-speed, 4M bit static RAMs organized as 512K words by 8 bits. It is fabricated using ISSI's high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When CS1 is HIGH (deselected) the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (WE) controls both writing and reading of the memory.

The IS62WV5128ALL and IS62WV5128BLL are packaged in the JEDEC standard 32-pin TSOP (TYPE I), 32-pin sTSOP (TYPE I), 32-pin TSOP (Type II), 32-pin SOP and 36-pin mini BGA.

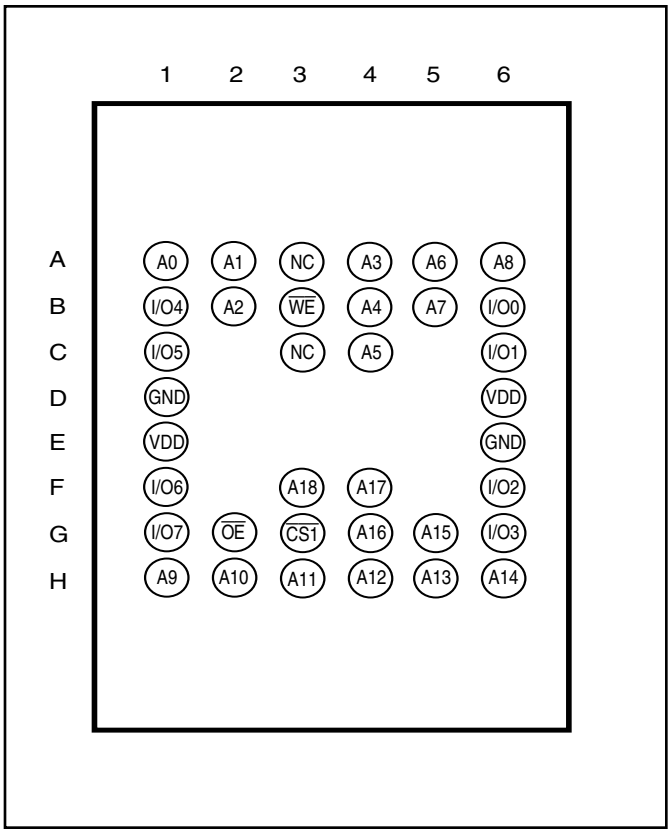
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

A0-A18	Address Inputs
CS1	Chip Enable 1 Input
OE	Output Enable Input
WE	Write Enable Input
I/O0-I/O7	Input/Output
NC	No Connection
V_{DD}	Power
GND	Ground

36-pin mini BGA (B) (6mm x 8mm) (Package Code B)

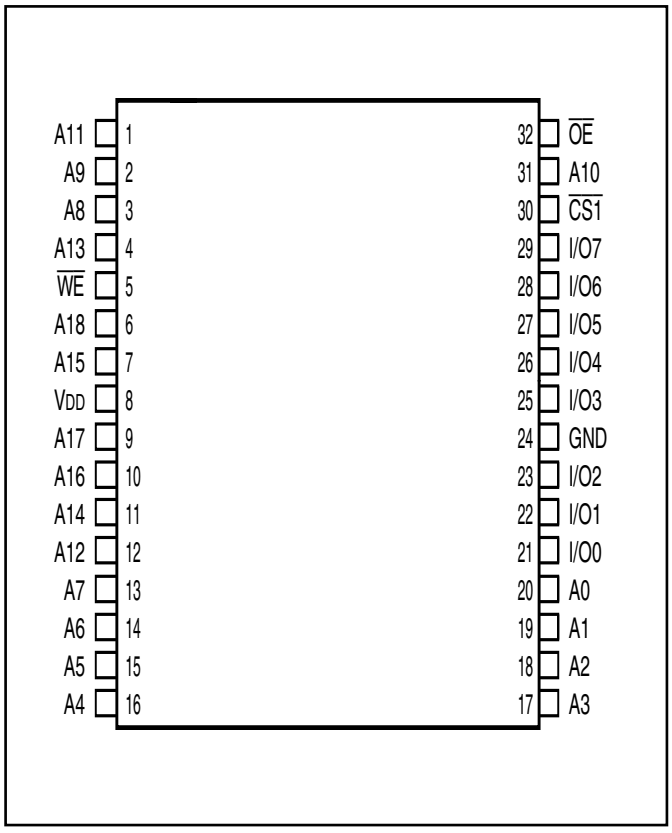


PIN DESCRIPTIONS

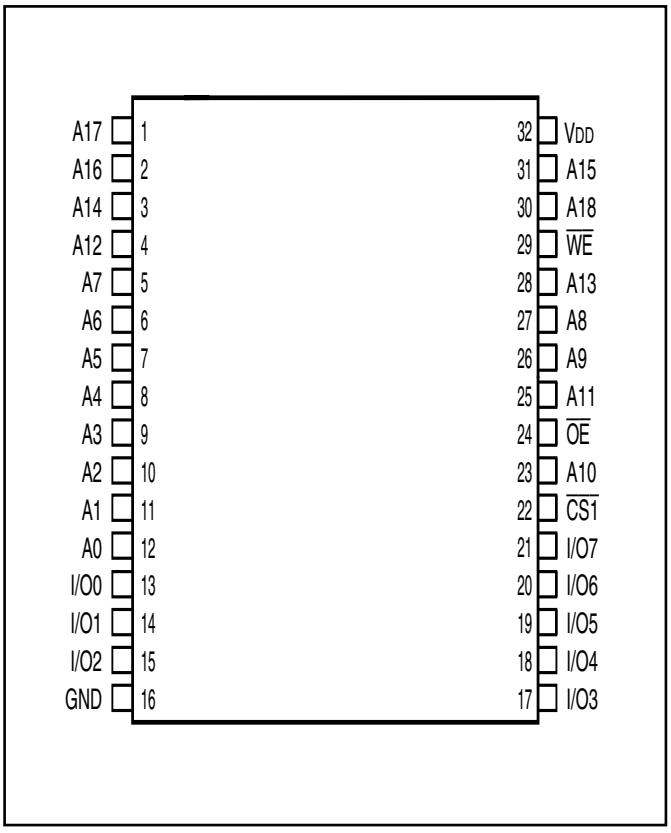
A0-A18	Address Inputs
CS1	Chip Enable 1 Input
OE	Output Enable Input
WE	Write Enable Input
I/O0-I/O7	Input/Output
VDD	Power
GND	Ground

PIN CONFIGURATION

32-pin TSOP (TYPE I), (Package Code T)
32-pin sTSOP (TYPE I) (Package Code H)



32-pin SOP (Package Code Q)
32-pin TSOP (TYPE II) (Package Code T2)



OPERATING RANGE (V_{DD})

Range	Ambient Temperature	IS62WV5128ALL	IS62WV5128BLL
Commercial	0°C to +70°C	1.65V - 2.2V	2.5V - 3.6V
Industrial	–40°C to +85°C	1.65V - 2.2V	2.5V - 3.6V

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.2 to V_{DD}+0.3	V
V_{DD}	V_{DD} Related to GND	–0.2 to V_{DD}+0.3	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.65-2.2V	1.4	—	V
		I_{OH} = -1 mA	2.5-3.6V	2.2	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	1.65-2.2V	—	0.2	V
		I_{OL} = 2.1 mA	2.5-3.6V	—	0.4	V
V_{IH}	Input HIGH Voltage		1.65-2.2V	1.4	V_{DD} + 0.2	V
			2.5-3.6V	2.2	V_{DD} + 0.3	V
V_{IL}[1]	Input LOW Voltage		1.65-2.2V	–0.2	0.4	V
			2.5-3.6V	–0.2	0.6	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		–1	1	µA

Notes:
1. V_{IL} (min.) = –1.0V for pulse width less than 10 ns.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	10	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	IS62WV5128ALL (Unit)	IS62WV5128BLL (Unit)
Input Pulse Level	0.4V to V_{DD}-0.2V	0.4V to V_{DD}-0.3V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V_{REF}	V_{REF}
Output Load	See Figures 1 and 2	See Figures 1 and 2

	IS62WV5128ALL 1.65 - 2.2V	IS62WV5128BLL 2.5V - 3.6V
R1(Ω)	3070	3070
R2(Ω)	3150	3150
V_{REF}	0.9V	1.5V
V_{TM}	1.8V	2.8V

AC TEST LOADS

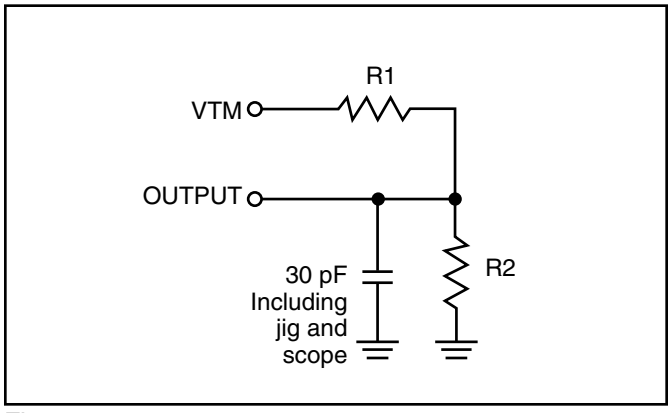


Figure 1

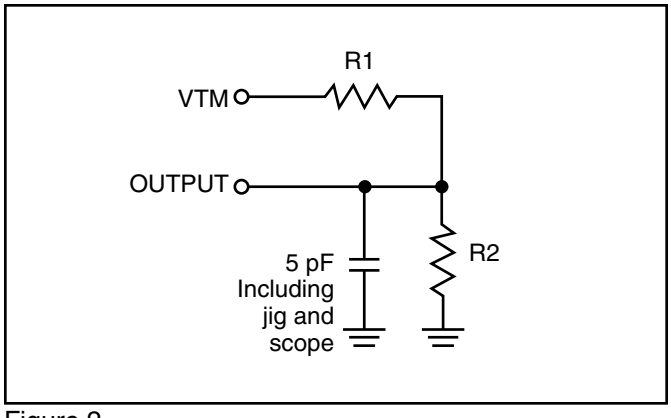


Figure 2

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

62WV5128ALL (1.65V - 2.2V)

Symbol	Parameter	Test Conditions		Max. 70 ns	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	25 30	mA
I_{CC1}	Operating Supply Current	V_{DD} = Max., CS1 = 0.2V WE = V_{DD}-0.2V f=1MHZ	Com. Ind.	10 10	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} CS1 = V_{IH}, f = 1 MHz	Com. Ind.	0.35 0.35	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., CS1 ≥ V_{DD} – 0.2V, V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com. Ind.	15 15	µA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

62WV5128BLL (2.5V - 3.6V)

Symbol	Parameter	Test Conditions		Max. 55 ns	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	40 45	mA
I_{CC1}	Operating Supply Current	V_{DD} = Max., CS1 = 0.2V WE = V_{DD}-0.2V f=1MHZ	Com. Ind.	15 15	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} CS1 = V_{IH}, f = 1 MHz	Com. Ind.	0.35 0.35	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., CS1 ≥ V_{DD} – 0.2V, V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com. Ind.	15 15	µA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

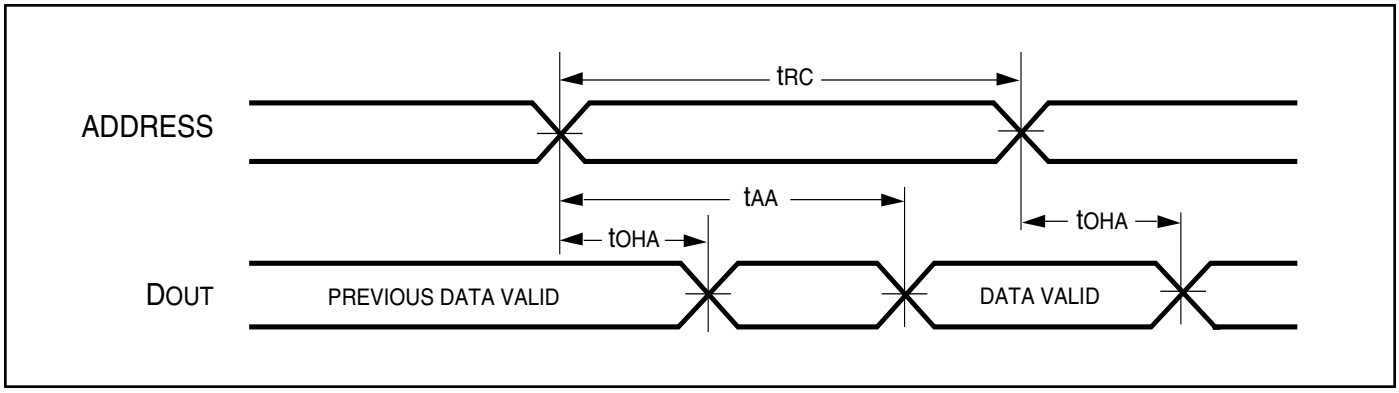
Symbol	Parameter	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	Unit
t_{RC}	Read Cycle Time	55	—	70	—	ns
t_{AA}	Address Access Time	—	55	—	70	ns
t_{OHA}	Output Hold Time	10	—	10	—	ns
t_{ACS1}	CS1 Access Time	—	55	—	70	ns
t_{DOE}	OE Access Time	—	25	—	35	ns
t_{HZOE}[2]	OE to High-Z Output	—	20	—	25	ns
t_{LZOE}[2]	OE to Low-Z Output	5	—	5	—	ns
t_{HZCS1}	CS1 to High-Z Output	0	20	0	25	ns
t_{LZCS1}	CS1 to Low-Z Output	10	—	10	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V_{DD}-0.2V/V_{DD}-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

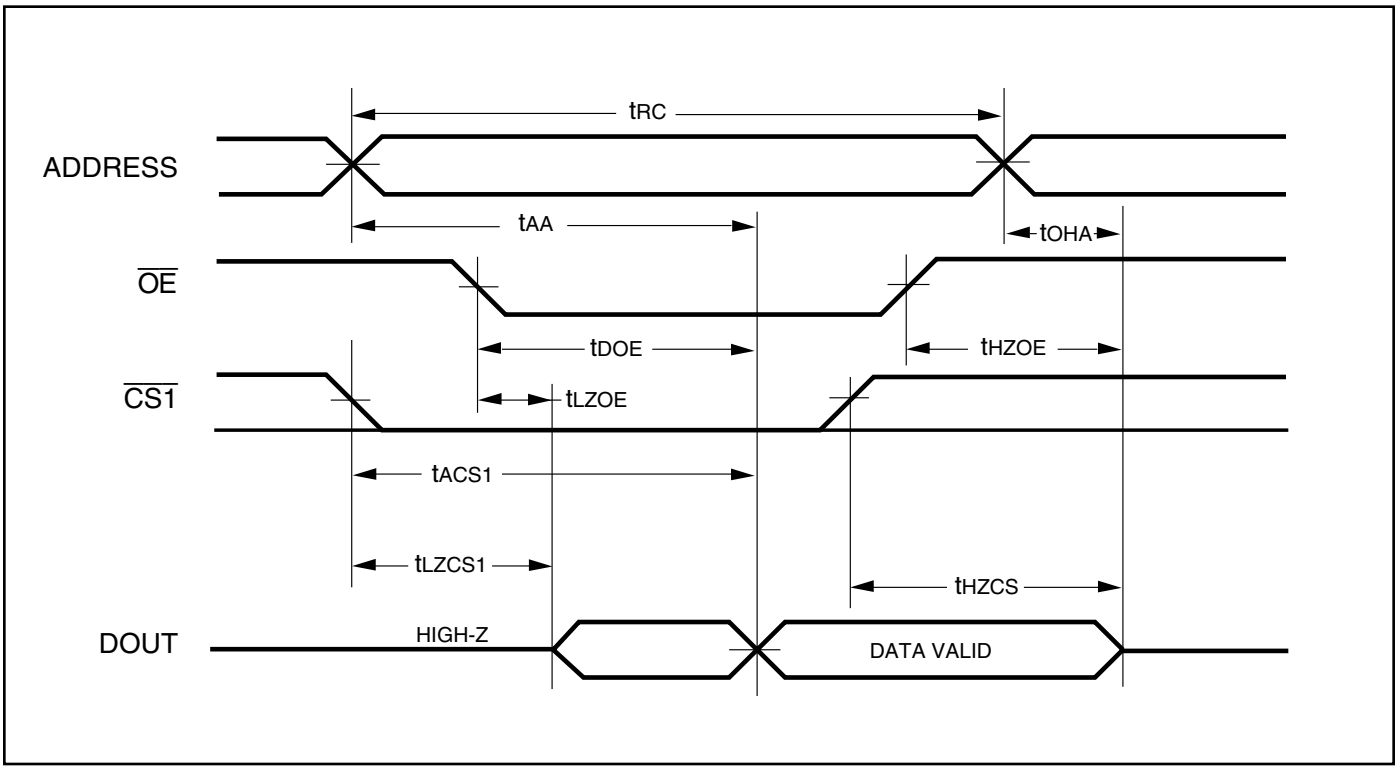
AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) (CS1 = OE = V_{IL}, WE = V_{IH})



AC WAVEFORMS

READ CYCLE NO. 2[1,3] (CS1, OE Controlled)



Notes:
1. WE is HIGH for a Read Cycle.
2. The device is continuously selected. OE, CS1= V_{IL}. WE=V_{IH}.
3. Address is valid prior to or coincident with CS1 LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

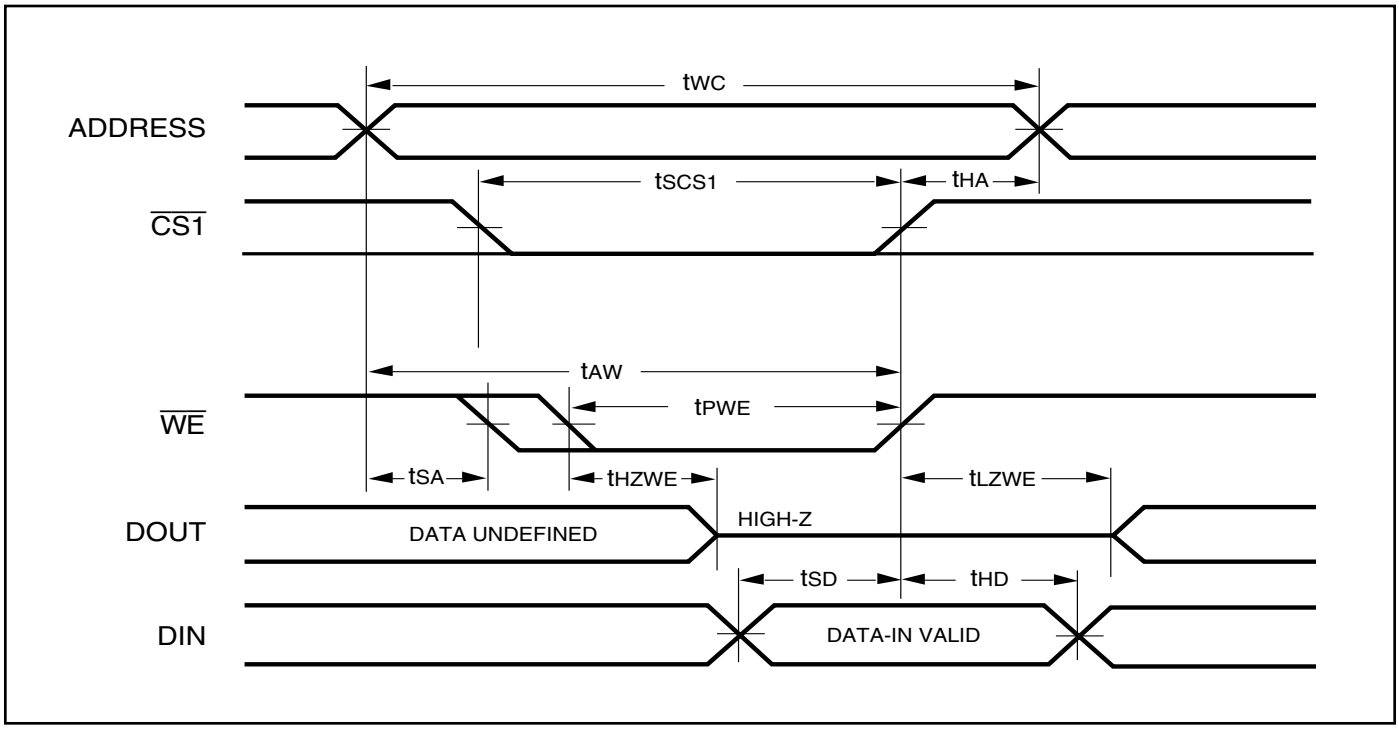
Symbol	Parameter	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	Unit
t_{WC}	Write Cycle Time	55	—	70	—	ns
t_{SCS1}	CS1 to Write End	45	—	60	—	ns
t_{AW}	Address Setup Time to Write End	45	—	60	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWE}	WE Pulse Width	40	—	50	—	ns
t_{SD}	Data Setup to Write End	25	—	30	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[3]	WE LOW to High-Z Output	—	20	—	20	ns
t_{LZWE}[3]	WE HIGH to Low-Z Output	5	—	5	—	ns

Notes:

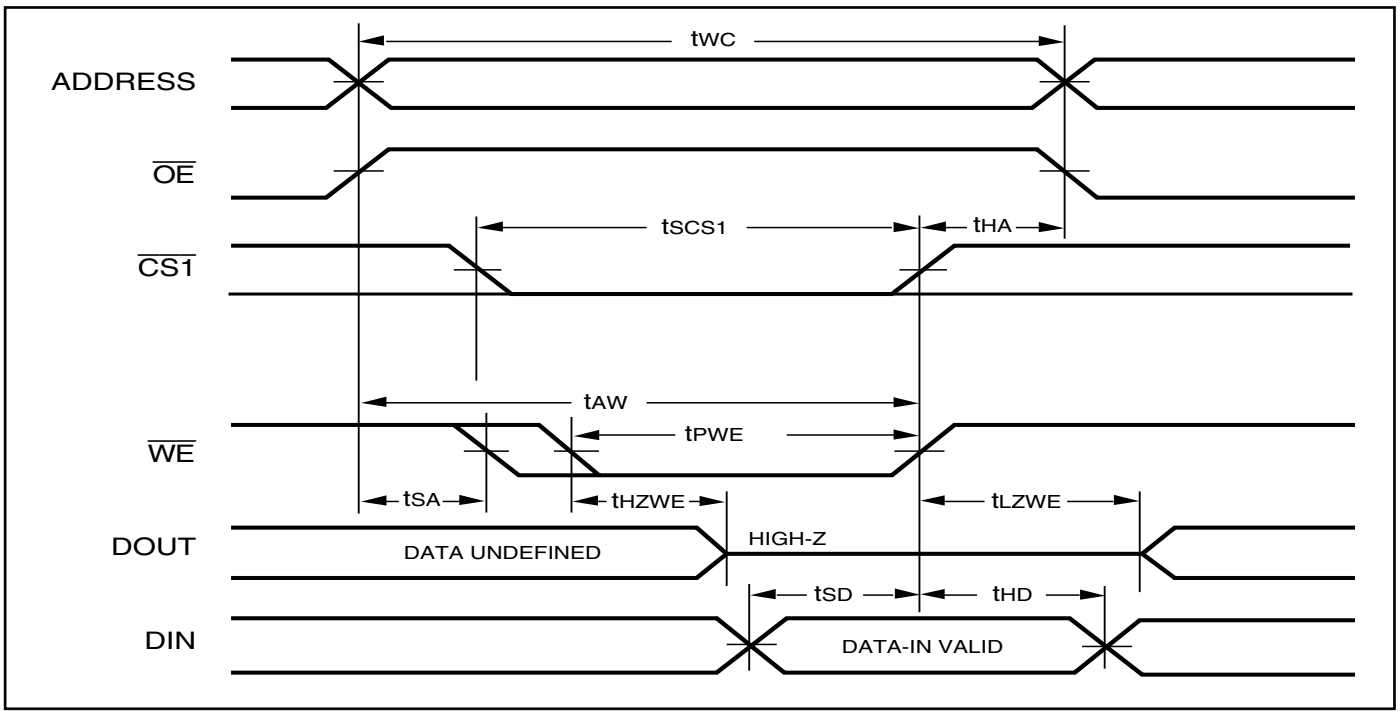
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4V to V_{DD}-0.2V/V_{DD}-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of CS1 LOW and WE LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

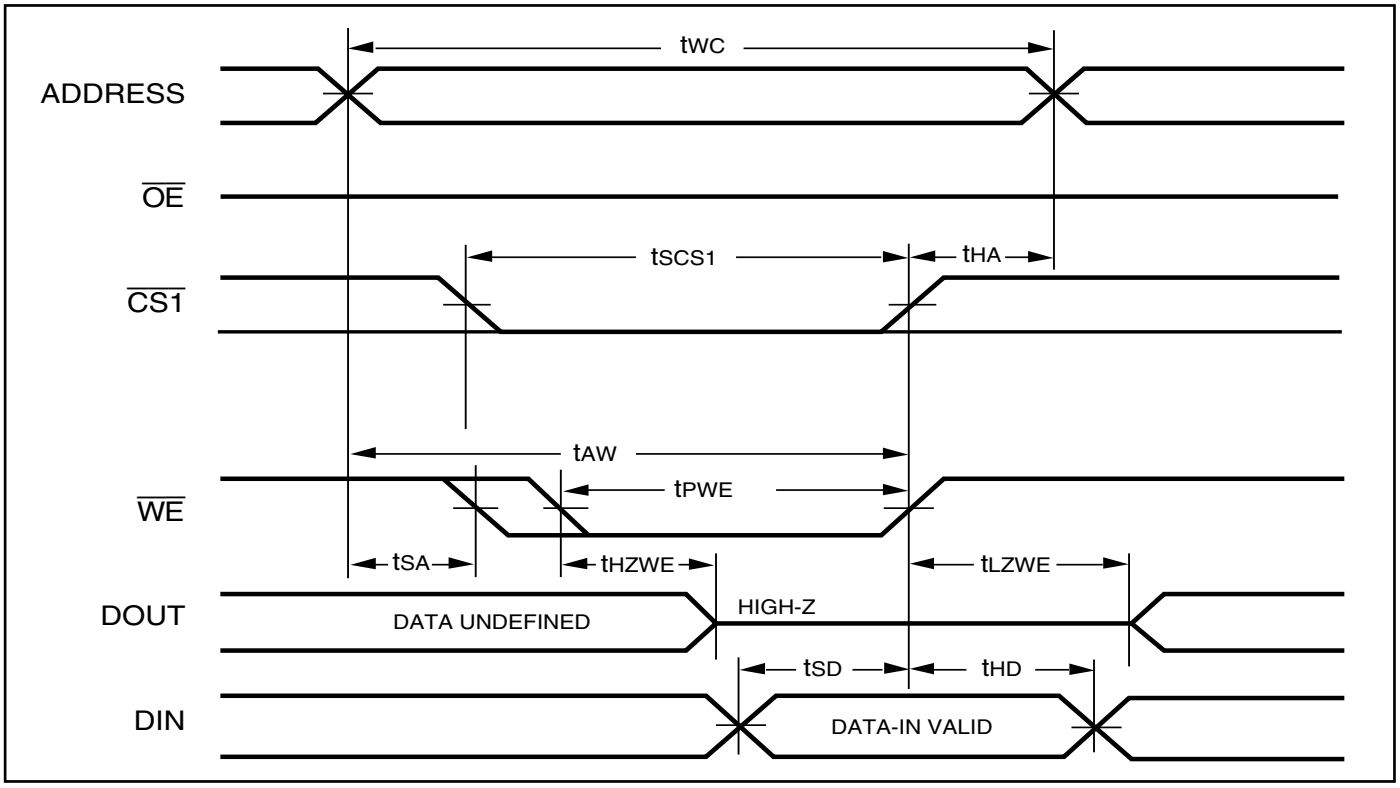
WRITE CYCLE NO. 1 (CS1 Controlled, OE = HIGH or LOW)



WRITE CYCLE NO. 2 (WE Controlled: OE is HIGH During Write Cycle)



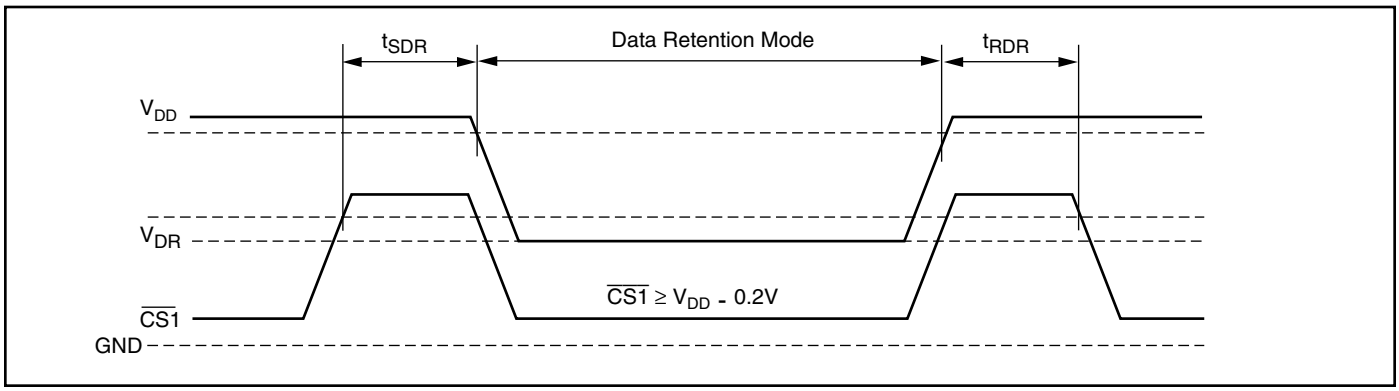
WRITE CYCLE NO. 3 (WE Controlled: OE is LOW During Write Cycle)



DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	1.2	3.6	V
I_{DR}	Data Retention Current	V_{DD} = 1.2V, CS1 ≥ V_{DD} – 0.2V	—	15	µA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	—	ns

DATA RETENTION WAVEFORM (CS1 Controlled)



ORDERING INFORMATION

IS62WV5128ALL (1.65V-2.2V)

Industrial Range: –40°C to +85°C

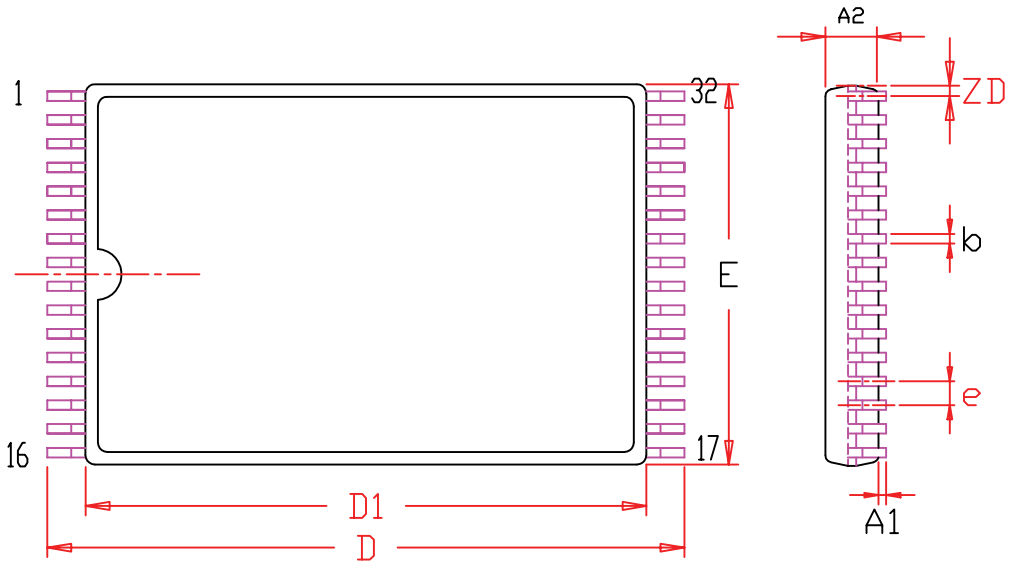
Speed (ns)	Order Part No.	Package
70	IS62WV5128ALL-70BI	mini BGA (6mmx8mm)

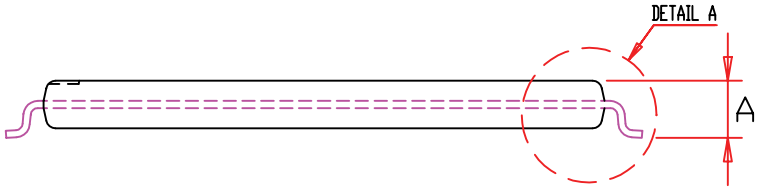
ORDERING INFORMATION

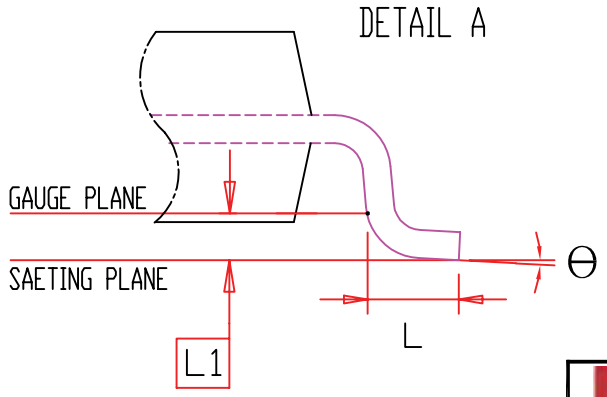
IS62WV5128BLL (2.5V - 3.6V)

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS62WV5128BLL-55TLI	TSOP, TYPE I, Lead-free
55	IS62WV5128BLL-55QLI	SOP, Lead-free
55	IS62WV5128BLL-55T2LI	TSOP, TYPE II, Lead-free
55	IS62WV5128BLL-55HLI	sTSOP, TYPE I, Lead-free
55	IS62WV5128BLL-55BI	mini BGA (6mmx8mm)
55	IS62WV5128BLL-55BLI	mini BGA (6mmx8mm), Lead-free







SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.95		1.25	0.037		0.049
A1	0.05		0.15	0.002		0.008
A2	0.90		1.05	0.035		0.041
b	0.16		0.27	0.006		0.011
D	13.10	13.40	13.70	0.516	0.528	0.539
D1	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	0.50 BSC.			0.020 BSC.		
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.25 BSC.			0.010 BSC.		
ZD	0.25 REF.			0.010 REF.		
Θ	0	3°	5°	0	3°	5°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
4. Reference Document : JEDEC MO-183

	TITLE	32L 8x13.4mm TSOP-1 Package Outline	REV.	E	DATE	04/24/2009

SYMBOL	DIMENSION IN MM		
	MIN	NOM	MAX
A	1.00		1.20
A1	0.05		0.20
A2	0.95	1.00	1.05
b	0.17		0.27
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	7.80	8.00	8.20
e		0.50 BSC.	
L	0.40		0.70
L1		0.25 BSC.	
ZD		0.25 REF.	
θ	0	5°	8°

NOTE :

1. Controlling dimension : mm
2. Dimension D1 adn E do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

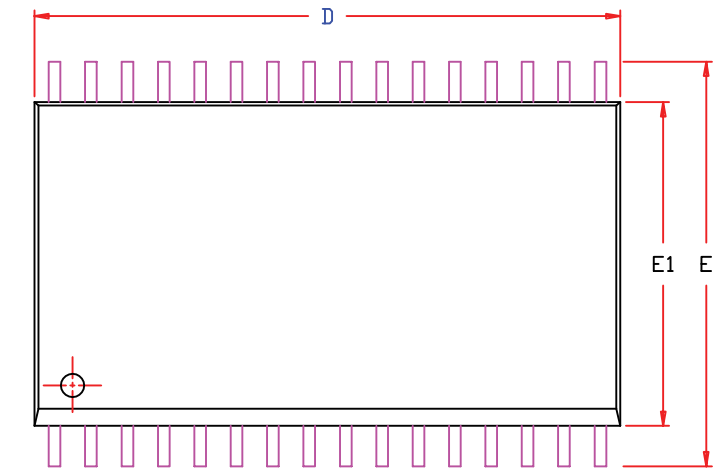
ISSI®	TITLE	32L 8x20mm TSOP-1 Package Outline	REV.	E	DATE	06/08/2006

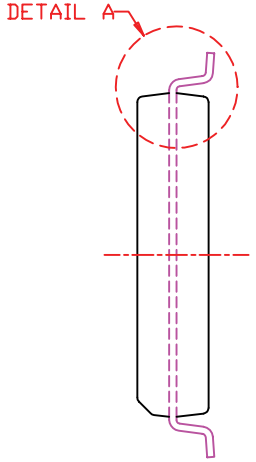
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	—	1.20	0.039	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	—	0.52	0.012	—	0.020
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e		1.27 BSC.			0.050 BSC.	
L	0.40	0.50	0.60	0.016	0.020	0.024
L1		0.25 BSC.			0.010 BSC.	
ZD		0.95 REF.			0.037 REF.	
θ	0	—	8°	0	—	8°

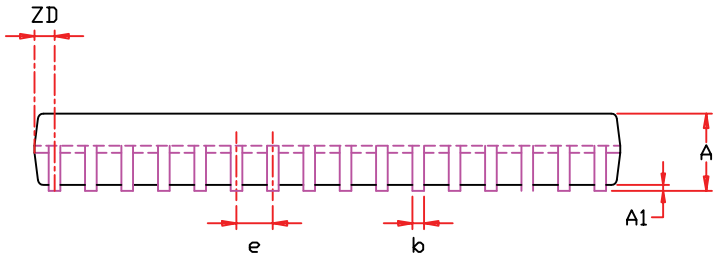
NOTE :

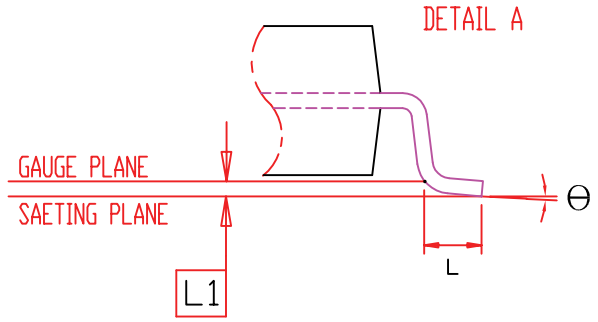
1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

TITLE	32L 400mil TSOP-2 Package Outline	REV.	E	DATE 06/23/2009







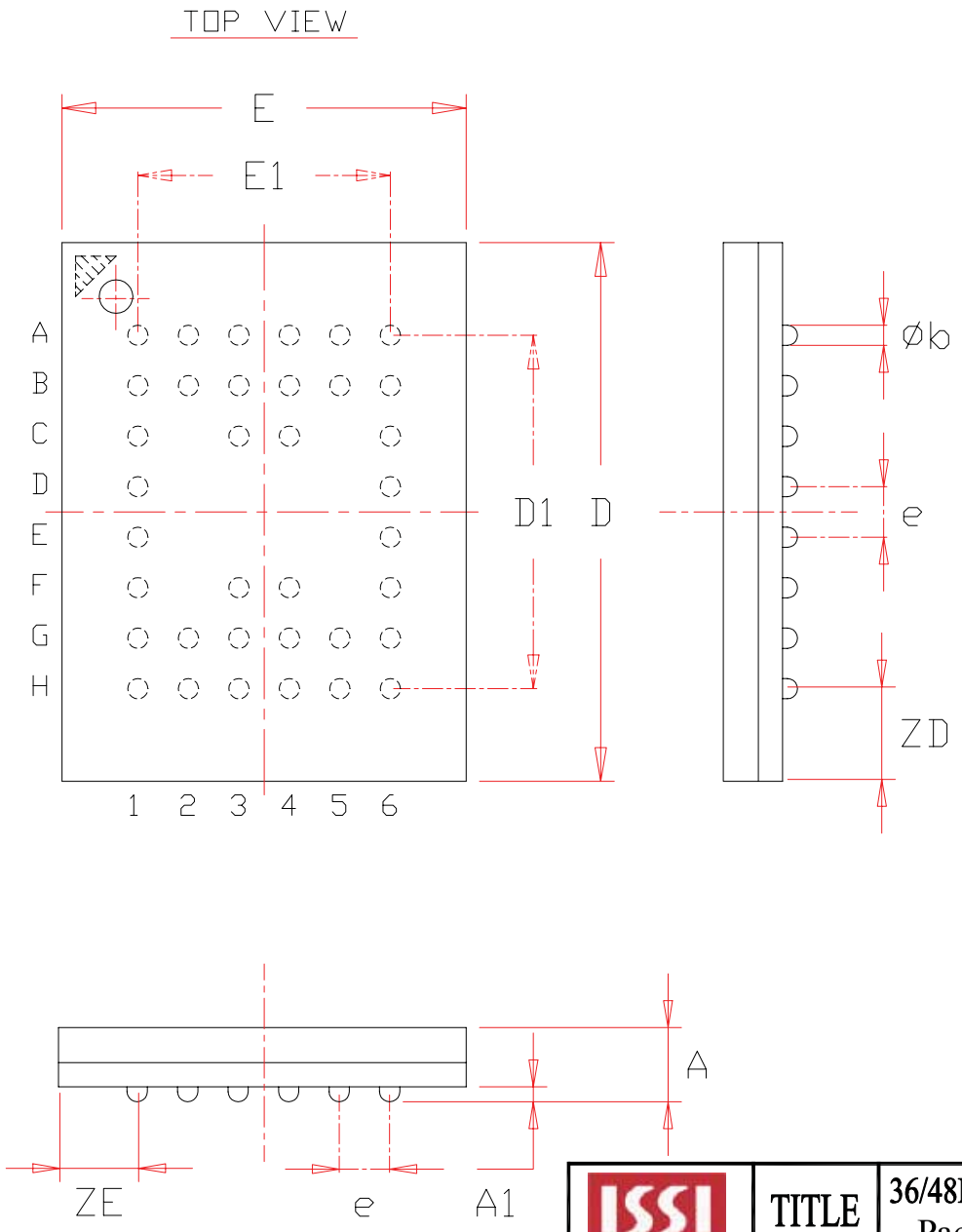


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.62	—	3.05	0.103	—	0.120
A1	0.05	—	0.30	0.002	—	0.012
b	0.33	—	0.51	0.013	—	0.020
D	20.24	—	20.75	0.797	—	0.817
E	13.79	—	14.45	0.543	—	0.569
E1	11.18	—	11.43	0.440	—	0.450
e	1.27 BSC.			0.050 BSC.		
L	0.38	—	1.27	0.015	—	0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.725 REF.			0.029 REF.		
θ	0	—	8°	0	—	8°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

ISSI	TITLE	32L 450mil SOP Package Outline	REV.	F	DATE	09/23/2013



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.20		0.30	0.008		0.012
Øb	0.30	0.35	0.40	0.012	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	5.25 BSC.			0.207 BSC.		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	3.75 BSC.			0.148 BSC.		
e	0.75 BSC.			0.030 BSC.		
ZD	1.375 REF.			0.054 REF.		
ZE	1.125 REF.			0.044 REF.		

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

ISSI	TITLE	36/48L 6x8mm TF-BGA Package Outline	REV.	E	DATE	08/12/2008